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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/710,510	07/16/2004	Elie Awad	BUR920030175US1	4509

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/710,510	AWAD ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6-11,14-18,21 and 22* is/are rejected.

7)☒ Claim(s) *4,5,12,13,19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/16/2004 is acceptable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. **Claims 1-2, 6-11, 14-17, and 21-22** are rejected under 35 U.S.C. 102(b) as being anticipated by Matsunaga et al. U.S. Patent 6,559,548 (the '548 reference).

The '548 reference discloses in Figs. 1 and 7's and respective portions of the specification a semiconductor structure and a method for forming thereof as claimed.

Referring to **claims 1 and 16**, the reference discloses a semiconductor structure and a method of forming thereof, comprising:

a substrate (10 or 10/11, Fig. 1; or 60 or 60/71, Fig. 7E);

a first layer (13; or 74 or 77) over said substrate, said first layer comprising a first material (SOG) having a first modulus of elasticity;

a first structure (12; or 76/75 or 79/78) formed within said first layer, said first structure having an upper surface; and

a stress diverting structure ("reinforcement insulating layer" 14; or 80 - column 4, lines 35-40; or column 9, lines 24-31) proximate said first structure, wherein said stress diverting structure provides a low mechanical stress region at said upper surface of said first structure when a physical load is applied to said first structure.

Referring to **claims 2 and 17**, the reference further discloses that said first structure comprises a conductor ("wiring" 12, 75, 78, plugs 76, 79).

Referring to **claim 9**, the reference discloses a semiconductor structure comprising:

a substrate (60, Fig. 7E);

an active device region (source/drain 62/63) embedded within said substrate;

a filler layer (74/77) over said substrate, said filler layer comprising a material (SOG) having a first modulus of elasticity;

a bondpad (84) over said filler layer, wherein said filler layer comprises a plurality of metal/via levels (75/78/76/79) formed upwardly from said active device region to said bondpad; and

a shield (80) configured over said active device region, wherein said shield comprises a material having a second modulus of elasticity different than said first modulus of elasticity (SOG filler layer 74/77 having a Young's modulus of less than 10 GPa, column 8, lines 63+, reinforcement silicon oxide layer 80, similar to reinforcement insulating layer 14, having a Young's modulus of 50 GPa or more, column 4, lines 35+) wherein said shield terminates at any of a first and second metal/via level above said substrate.

Referring to **claims 6, 21, 10, and 14**, although not explicitly disclosed, said low mechanical stress region comprises stress values at levels below stress values in areas in said semiconductor structure unprotected by said stress diverting structure and said shield provides a low mechanical stress region on said active device region when a physical load is applied to said active device region.

Referring to **claims 7 and 22**, the reference further discloses that said first structure (12; or 76/75 or 79/78) is formed adjacent to said first layer (13; or 74 or 77).

Referring to **claims 8 and 15**, although the reference's figures do not explicitly show in a three dimensional view, one of ordinary skill in the art could realize that said stress diverting structure (14; or 80) is cubical and said shield (80) is cubical.

Referring to **claim 11**, as detailed above, said shield comprises a material having a modulus of elasticity (50 GPa or more) higher than said first modulus of elasticity (less than 10 GPa).

Claim Rejections - 35 USC § 102 & 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. **Claims 3 and 18** are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Matsunaga et al. U.S. Patent 6,559,548 (the '548 reference).

The '548 reference discloses a semiconductor structure and a method for forming thereof as claimed or substantially as claimed. The difference between the claimed invention and the reference is a claimed function and an implicit disclosure for the Young's modulus for the BPSG layer 71. Specifically, with reference to **claims 3 and 18**, the reference discloses a semiconductor structure and a method of forming thereof, comprising:

a substrate (60, Fig. 7E);

a first layer (71, Fig. 7E) over said substrate, said first layer comprising a first material (BPSG) having a first modulus of elasticity;

a first structure (73/72) formed within said first layer, said first structure having an upper surface; and

a structure (SOG layer 74) proximate said first structure;

wherein said structure (74) comprises a second material (SOG) and is selectively formed over said upper surface of said first structure (73/72).

However, the reference fails to explicitly disclose that the structure 74 is a stress diverting structure for diverting mechanical stress when a physical load is applied to said first structure; and further fails to explicitly disclose that said second material has a second modulus of elasticity less than said first modulus of elasticity.

Nevertheless, although the reference fails to explicitly disclose a value for the first modulus of elasticity, the reference explicitly disclose, as detailed above, that the second

modulus elasticity for the second material (SOG) is deliberately low for higher speed operation (column 9). Since the second modulus elasticity is deliberately low, there appears that the first modulus elasticity is not low; or in other words, said second material appears to have a second modulus of elasticity less than said first modulus of elasticity. And, since the second material appears to have a second modulus of elasticity less than said first modulus of elasticity, the second material, which constitutes the structure 74, appears to constitute the claimed function of being a stress diverting structure.

Allowable Subject Matter

4. Claims 4, 5, 12, 13, 19, and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a semiconductor structure and a method for forming thereof having all exclusive limitations as recited in claims 1/4 (claims 1 and 4), 1/5, 9/12, 9/13, 16/19, and 16/20, characterized in the limitations of claims 4, 5, 12, 13, 19, and 20 respectively, in consideration with the respective independent claims.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
May 10, 2005